LEVEL SHIFT CIRCUIT

BACKGROUND OF THE INVENTION

The present invention relates to a level shift circuit functioning as an interface between circuits operating at different power supply voltages.

In a conventional level shift circuit having a CMOS configuration, a p-MOS transistor and an n-MOS transistor connected in series and interposed between the power supply and the ground inevitably turn ON at the same time at the transition of a data input and, as a result, feed-through current occurs at this time (see Japanese Laid-Open Publication No. 11-136120).

An LCD driver needs level shift circuits in the number obtained by multiplying the number of outputs by the number of bits. For example, an LCD driver having 8 bits and 384 outputs uses as many as 3072 level shift circuits. An application in which such a large number of level shift circuits are used has a drawback of increased power consumption caused by feed-through current in each of the level shift circuits and also has a drawback of a system malfunction occurring when an increase in the ground potential caused by the feed-through current is output as a noise to the outside of the chip.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to prevent the occurrence of feed-through current in a level shift circuit having a CMOS configuration.

In order to achieve this object, according to the present invention, adopted is a level shift circuit including: a level shift basic circuit for translating an input signal to an output signal which has a difference of a voltage between a first power supply and a second power supply having a lower voltage than that of the first power supply; and a control circuit

including a first circuit for disconnecting a feed-through current path in said level shift basic circuit between the first power supply and the second power supply in response to a first control input, and a second circuit for fixing a voltage of an output node from which the output signal is output in response to a second control input.

The control circuit includes: a first circuit for disconnecting a feed-through current path between the first power supply and the second power supply; and a second circuit for fixing a voltage of the output node while the first circuit disconnects the feed-through current path, and is configured such that the disconnection of the feed-through current path by the first circuit is canceled after the fixing of the voltage by the second circuit has terminated and the input signal transitions while the first circuit disconnects the feed-through current path.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a circuit diagram showing an example of a configuration of a level shift circuit according to the present invention.

FIG. **2** is a time chart showing an example of operation of the level shift circuit shown in FIG. **1**.

FIG. **3** is a circuit diagram showing a modified example of the level shift circuit shown in FIG. **1**.

FIG. **4** is a circuit diagram showing another example of the configuration of the level shift circuit of the present invention.

FIG. **5** is a time chart showing an example of operation of the level shift circuit shown in FIG. **4**.

FIG. **6** is a block diagram showing a modified example of the level shift circuit shown in FIG. **4**.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, embodiments of the present invention will be described with reference to the drawings.

FIG. **1** shows an example of a configuration of a level shift circuit according to the present invention. In FIG. **1**, reference numeral **10** denotes a level shift basic circuit having a CMOS configuration and reference numeral **20** denotes a control circuit for preventing feed-through current. The level shift basic circuit **10** includes two n-MOS transistors **M1** and **M2** and two p-MOS transistors **M3** and **M4**. The control circuit **20** includes two p-MOS transistors **M5** and **M6** and two n-MOS transistors **M7** and **M8**. Reference signs **Vin1** and **Vin2** denote complementary data inputs, reference signs **VS1** and **VS2** respectively denote control inputs, reference signs **Vout1** and **Vout2** respectively denote data outputs, reference sign **VDD** denotes a first power supply, and reference sign **VSS** denotes a second power supply (ground: 0V) having a voltage lower than VDD.

In FIG. **1**, Vin1 and Vin2 are connected to the gates of the n-MOS transistors **M1** and **M2**, respectively. The source of the n-MOS transistor **M1** is connected to the drain of the n-MOS transistor **M7** whose gate is connected to VS1. The source of the n-MOS transistor **M7** is connected to VSS. In the same manner, the source of the n-MOS transistor **M2** is connected to the drain of the n-MOS transistor **M8** whose gate is connected to VS1. The source of the n-MOS transistor **M8** is connected to VSS. The drain of the n-MOS transistor **M1** is connected to the drain of the p-MOS transistor **M3**. The drain of the n-MOS transistor **M2** is connected to the drain of the p-MOS transistor **M4**. The sources of the p-MOS transistors **M3** and **M4** are respectively connected to VDDs. The gate of the p-MOS transistor **M3** is connected to the drain of the p-MOS transistor **M4** at a connection point, which will be referred to as a first data output node

Vout1. The gate of the p-MOS transistor **M4** is connected to the drain of the p-MOS transistor **M3** at a connection point, which will be referred to as a second data output node **Vout2**. The sources of the p-MOS transistors **M5** and **M6** whose respective gates are connected to VS2 are respectively connected to VDDs. The drain of the p-MOS transistor **M5** is connected to Vout1, whereas the drain of the p-MOS transistor **M6** is connected to Vout2.

FIG. **2** shows an example of operation of the level shift circuit shown in FIG. **1**. First, as an initial state, VS1 and VS2 are at H levels, Vin1 is at an L level and Vin2 is at an H level. In this state (output period), Vout1 outputs VSS and Vout2 outputs VDD. Since the n-MOS transistor **M1** and the p-MOS transistor **M4** are OFF, no feed-through current flows between VDDs and VSSs.

Next, to switch the level shift outputs, the transitions of Vin1 and Vin2 are made in a period in which the n-MOS transistors **M7** and **M8** for control are turned OFF by changing VS1 to an L level (switch-off period). During this switch-off period, the sources of the n-MOS transistors **M1** and **M2** are respectively disconnected from VSSs. In addition, in the switch-off period, VS2 is changed to an L level so that the p-MOS transistors **M5** and **M6** for control turn ON. While the control p-MOS transistors **M5** and **M6** are ON, Vout1 and Vout2 are both precharged to VDD (precharge period). Accordingly, Vout1 transitions from VSS to VDD at the beginning of the precharge period.

In the example shown in FIG. **2**, after Vin1 and Vin2 transition from the L level to the H level and from the H level to the L level, respectively, and then the precharge period terminates by returning VS2 to the H level, Vout2 transitions from VDD to VSS at the point of time when the disconnections by the n-MOS transistors **M7** and **M8** are canceled by returning VS1 to the H level.

During the switching of the level shift output described above, the n-MOS transistor **M1** and the p-MOS transistor **M3** do not turn ON at the same time, and the n-MOS transistor **M2** and the p-MOS transistor **M4** also do not turn ON at the same time. Accordingly, no feed-through current flows through these transistors. While Vout1 and Vout2 output VDD due to turning ON of the control p-MOS transistors **M5** and **M6**, the sources of the n-MOS transistors **M1** and **M2** are respectively disconnected from VSSs by the control n-MOS transistors **M7** and **M8**. As a result, no feed-through current flows through the control p-MOS transistors **M5** and **M6**.

Assuming that the level shift circuit shown in FIG. **1** does not include the control circuit **20**, when Vin1 and Vin2 transition from the L level to the H level and from the H level to the L level, respectively, the n-MOS transistor **M1** changes from the OFF-state to the ON-state and the n-MOS transistor **M2** changes from the ON-state to the OFF-state. In this case, both the n-MOS transistor **M1** and the p-MOS transistor **M3** are ON, so that feed-through current occurs between VDDs and VSSs. To prevent this feed-through current, conventionally, the current driving capability (gate width) of the n-MOS transistor **M1** in the ON-state has been designed higher than that of the p-MOS transistor **M3** such that the potential of Vout2 is gradually reduced by the n-MOS transistor **M1** and eventually the feed-through current is shut off. In the same manner, the current driving capability (gate width) of the n-MOS transistor **M2** in the ON-state has been designed higher than that of the p-MOS transistor **M4**. On the other hand, in the level shift circuit shown in FIG. **1** and provided with the control circuit **20** for preventing feed-through current, it is unnecessary for the n-MOS transistors **M1** and **M2** to shut off the feed-through current. Therefore, the current driving capabilities (gate widths) of the n-MOS transistors **M1** and **M2** are not necessarily higher than those of the p-MOS transistors **M3** and **M4**. Accordingly, the circuit area of the level shift basic circuit **10** can be reduced.

In FIG. **1**, the level shift circuit is configured such that Vout1 and Vout2 are fixed at VDD by the p-MOS transistors **M5** and **M6** in accordance with VS2. Alternatively, Vout1 and Vout2 may be fixed at VSS in accordance with the polarity of a required output node. However, the fixing at VDD has the advantage of smaller size of the n-MOS transistors **M1** and **M2** because the p-MOS transistors M3 and **M4** are OFF both at the falling edge of Vout1 and at the falling edge of Vout2.

In addition, the control n-MOS transistors **M7** and **M8** shown in FIG. **1** may be replaced with one n-MOS transistor. However, in terms of a layout, the two n-MOS transistors **M7** and **M8** are preferably adopted.

FIG. **3** shows a modified example of the level shift circuit shown in FIG. **1**. In FIG. **3**, one control circuit **20** for preventing feed-through current is provided for n level shift basic circuits **10** where n is an integer of two or more. Then, the area penalty due to provision of the control circuit **20** can be reduced.

FIG. **4** shows another example of the configuration of the level shift circuit of the present invention. In FIG. **4**, reference numeral **10** denotes a level shift basic circuit having a CMOS configuration, and reference numeral **21** denotes a control circuit for preventing feed-through current. The level shift basic circuit **10** includes two n-MOS transistors **M1** and **M2** and two p-MOS transistors **M3** and **M4**. The control circuit **21** includes two two-input NOR circuits **N1** and **N2** and two p-MOS transistors **M5** and **M6**. Reference signs **Vin1** and **Vin2** denote complementary data inputs, reference signs **VS1** and **VS2** respectively denote control inputs, reference signs **Vout1** and **Vout2** respectively denote data outputs, reference sign **VDD** denotes a first power supply, and reference sign **VSS** denotes a second power supply (ground: 0V) having a voltage lower than VDD.

In FIG. **4**, the NOR circuit **N1** receives Vin1 and VS1, and the NOR circuit **N2** receives Vin2 and VS1. The gate of the n-MOS transistor **M1** is connected to an output

V1 of the NOR circuit **N1**, and the gate of the n-MOS transistor **M2** is connected to an output **V2** of the NOR circuit **N2**. The sources of the n-MOS transistors **M1** and **M2** are respectively connected to VSSs. The drain of the n-MOS transistor **M1** is connected to the drain of the p-MOS transistor **M3**, and the drain of the n-MOS transistor **M2** is connected to the drain of the p-MOS transistor **M4**. The sources of the p-MOS transistors **M3** and **M4** are respectively connected to VDDs. The gate of the p-MOS transistor **M3** is connected to the drain of the p-MOS transistor **M4** at a connection point, which will be referred to as a first data output node **Vout1**. The gate of the p-MOS transistor **M4** is connected to the drain of the p-MOS transistor **M3** at a connection point, which will be referred to as a second data output node **Vout2**. The sources of the p-MOS transistors **M5** and **M6** whose respective gates are connected to VS2 are respectively connected to VDDs. The drain of the p-MOS transistor **M5** is connected to Vout1, whereas the drain of the p-MOS transistor **M6** is connected to Vout2.

FIG. **5** shows an example of operation of the level shift circuit shown in FIG. **4**. First, as an initial state, VS1 is at an L level, VS2 is at an H level, Vin1 is at an L level and Vin2 is at an H level. In this state (output period), V1 is at an H level, V2 is at an L level, Vout1 outputs VDD and Vout2 outputs VSS. Since the n-MOS transistor **M2** and the p-MOS transistor **M3** are OFF, no feed-through current flows between VDDs and VSSs.

Next, to switch the level shift outputs, transitions of Vin1 and Vin2 are made in a period in which VS1 is changed to an H level and thereby the gate voltages **V1** and **V2** of the n-MOS transistors **M1** and **M2** are reduced to L levels so that the n-MOS transistors **M1** and **M2** are forced to turn OFF (switch-off period). In addition, in this switch-off period, VS2 is changed to an L level so that the p-MOS transistors **M5** and **M6** for control turn ON. In a period during which the control p-MOS transistors **M5** and **M6** are ON, both Vout1 and Vout2 are precharged to VDD (precharge period). Accordingly, Vout2

transitions from VSS to VDD at the beginning of the precharge period.

In the example shown in FIG. **5**, after Vin1 and Vin2 transition from the L level to the H level and from the H level to the L level, respectively, and then the precharge period terminates by returning VS2 to the H level, V2 transitions from the L level to the H level and Vout1 transitions from VDD to VSS at the point of time when the forced OFF-states of the n-MOS transistors **M1** and **M2** are canceled by returning VS1 to the L level.

During the switching of the level shift output described above, the n-MOS transistor **M1** and the p-MOS transistor **M3** do not turn ON at the same time, and the n-MOS transistor **M2** and the p-MOS transistor **M4** also do not turn ON at the same time. Accordingly, no feed-through current flows through these transistors. While turning ON of the control p-MOS transistors **M5** and **M6** makes Vout1 and Vout2 output VDD, the n-MOS transistors **M1** and **M2** are in the forced OFF-states. Accordingly, no feed-through current flows through the control p-MOS transistors **M5** and **M6**.

In the level shift circuit shown in FIG. **4** and provided with the control circuit **21** for preventing feed-through current, also, the current driving capabilities (gate widths) of the n-MOS transistors **M1** and **M2** are not necessarily higher than those of the p-MOS transistors **M3** and **M4**, either. Accordingly, the circuit area of the level shift basic circuit **10** can be reduced.

FIG. **6** shows a modified example of the level shift circuit shown in FIG. **4**. In FIG. **6**, one control circuit **22** for preventing feed-through current is provided for n level shift basic circuits **10** where n is an integer of two or more. Then, the area penalty due to provision of the control circuit **22** can be reduced.

Inverters may be appropriately added to an output stage of the level shift basic circuit **10** in the above embodiments depending on whether the subsequent circuit is a p-channel type or an n-channel type. In the above description, the second power supply is

VSS (=0V), but may be changed to a positive or negative power supply.

As described above, according to the present invention, it is possible to prevent the occurrence of feed-through current in a level shift circuit having a CMOS configuration. The inventive level shift circuit is useful as a level shift circuit functioning as an interface between circuits operating at different power supply voltages.